PROJECT REPORT

**Designing a down-conversion mixer using 65 nm CMOS technology and E-sim software.**

**Introduction**

This presentation discusses the design and performance of a down-conversion Gilbert cell mixer, focusing on its implementation using 65 nm CMOS technology in E-sim software.

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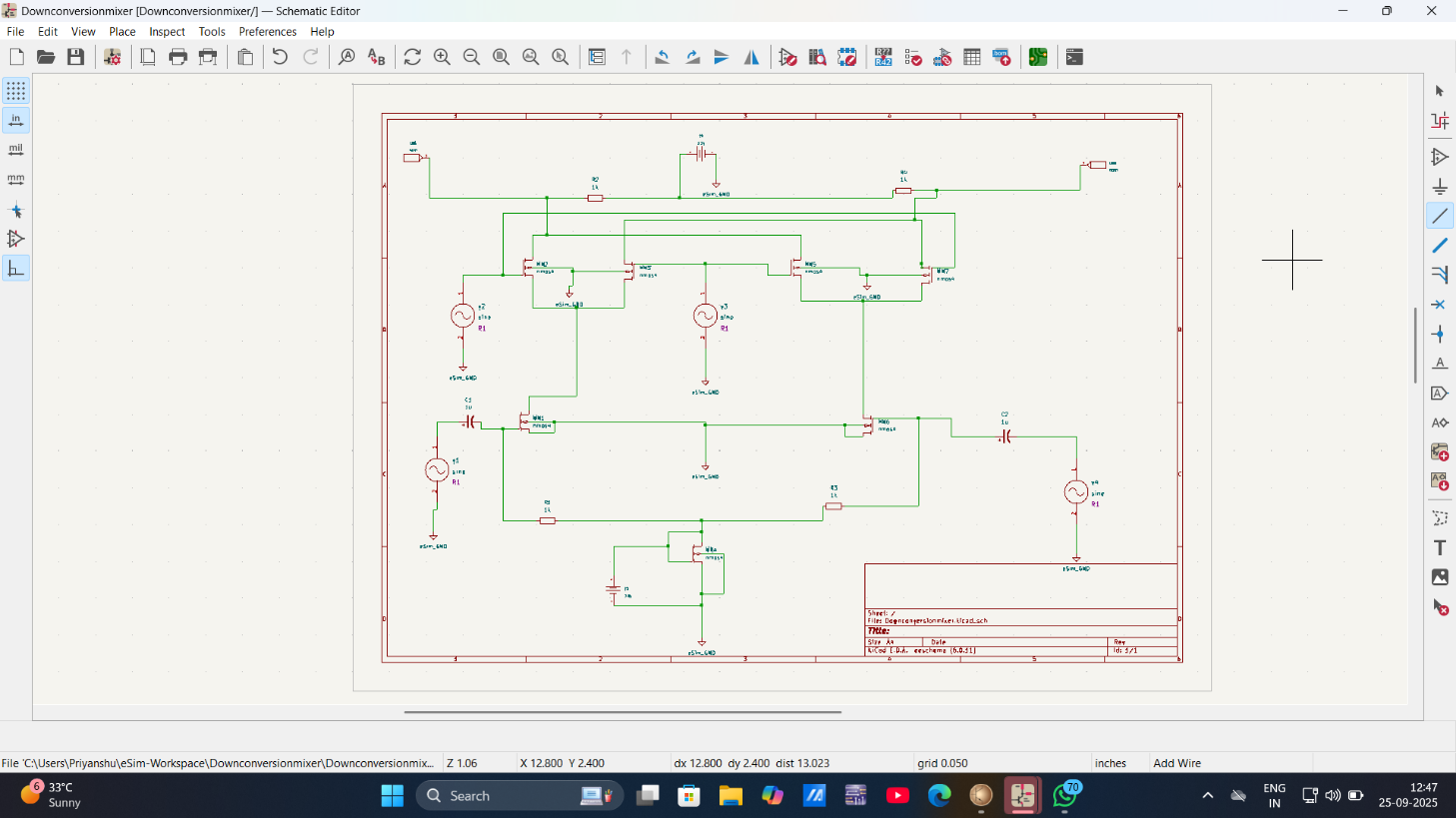
**Gilbert Cell Mixers proposed Circuit**

The Gilbert cell mixer is a crucial component in communication systems, providing efficient down-conversion of RF signals. It operates by using a double-balanced configuration that achieves high gain with low distortion, making it suitable for various applications, including RF and microwave circuits.

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**CMOS Technology Utilization**

Utilizing 65 nm CMOS technology allows for compact circuit design and reduced power consumption. This technology enhances performance metrics such as gain and linearity, making it optimal for the development of the proposed down-conversion mixer.



**Down-Conversion Mixer Design Woking**

1. **Transconductance Stage (Voltage-to-Current Conversion)**
2. **Transistors M2 and M3** are the core of the transconductance stage.
3. The **RF input signal (Radio Frequency**) is applied here.
4. These transistors **convert the RF voltage signal into a differential** current signal (±IRF).
5. This current is the **"**linear" signal that will be modulated by the local oscillator (LO).

#### 2. Switching Stage (Multiplication with LO Signal)

•**Transistors M4 to M7** form the **differential switching quad**.

•A **Local Oscillator (LO) signal** is applied differentially across these transistors.

•The function of this stage is to **multiply the RF current signal with the LO signal**, effectively mixing the two frequencies.

• When the LO signal toggles the switching transistors, it causes the

RF current from M2 and M3 to be **steered alternately between M4–M7 and M5–M6**.

• This switching mimics a **square-wave multiplication**, which is an efficient approximation of mixing in analog circuitry.

**3. Load Stage (Current-to-Voltage Conversion)**

•The **load resistors (Rd)** at the drains of the switching transistors convert the modulated (mixed) current into a voltage.

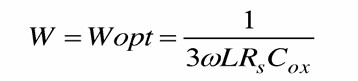
•This stage produces the **differential Intermediate Frequency (IF) output**.

•The IF signal contains components of the sum and difference frequencies (RF ± LO), where usually a lowpass filter extracts the desired difference frequency (IF).

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**Design Analysis**

1. Mixer design is based on optimizing transistor width to minimize noise.
2. Optimal transistor width:



where Cox = gate oxide capacitance per unit area, Rs = 50Ω. Operating frequency: 1.9 GHz, giving ω = 11.932 x 10⁹ rad/s.

1. Gate oxide capacitance: Cox = (Kox \* ε₀) / tox = 1.941 × 10⁻⁵ F/m²
2. Gate oxide thickness: tox = 17.77 nm, Kox ≈ 3.9, ε₀ =
3. 8.854×10⁻¹² F/m.

**Design Continuation**

Transistor Operating Region

1. All transistors must operate in saturation:

saturation region for optimal performance

1. Saturation ensures:
2. High gain
3. Stable current with respect to VDS

Saturation condition:

**VDS ≥ VGS − VT**

**Current & Transconductance Equations**

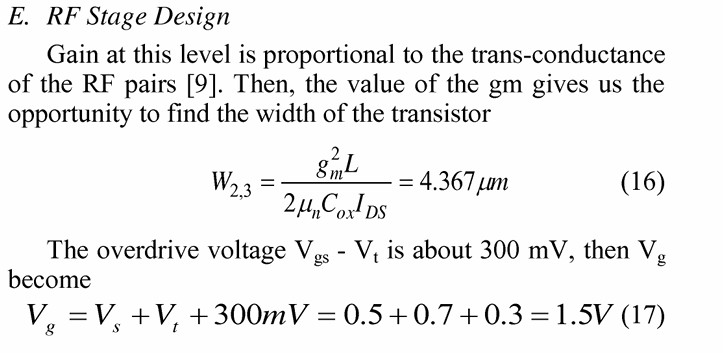
1. NMOS drain current in

![](data:application/octet-stream;base64,)

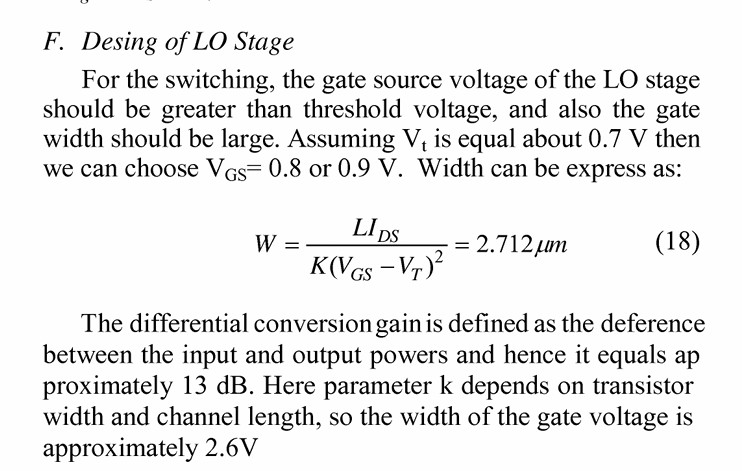
1. Transconductance (gm)

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RF part Design Continuation

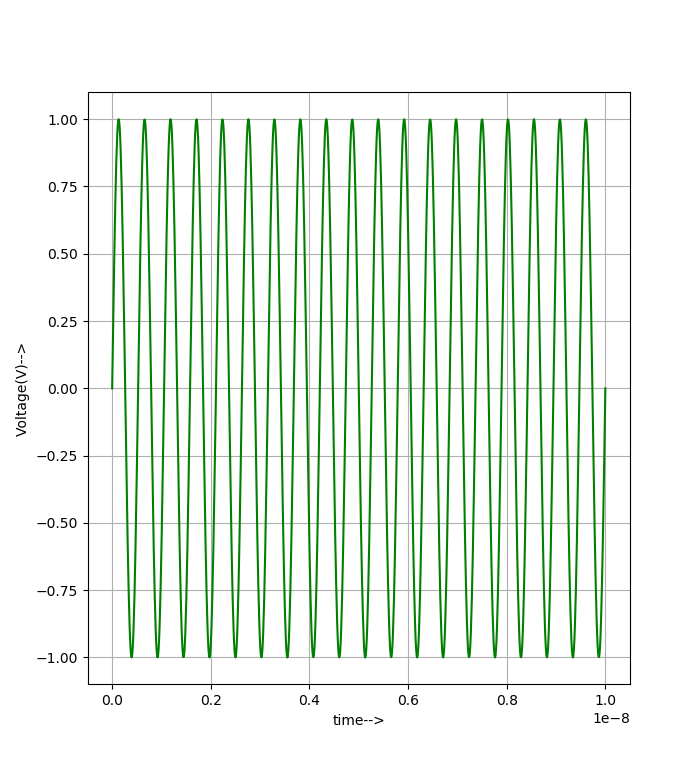


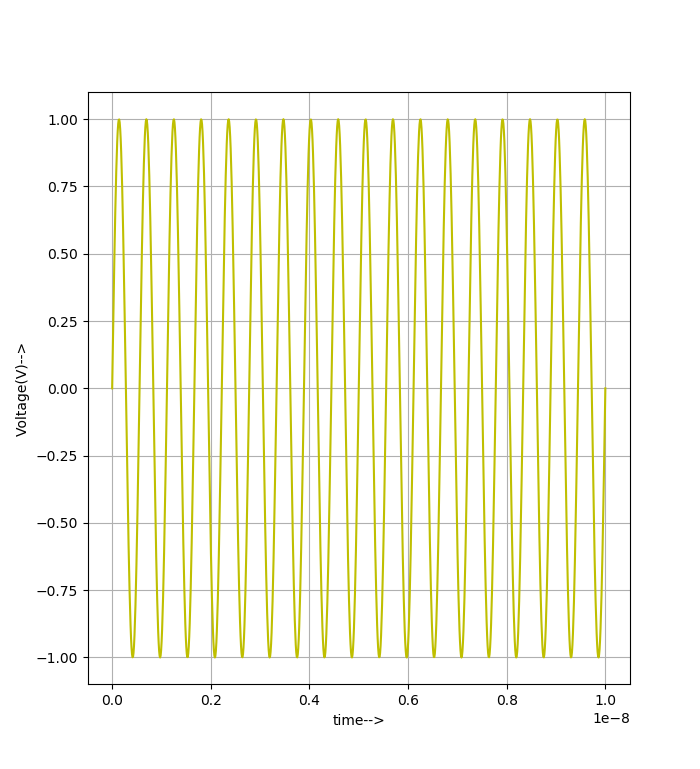
LO part Design Continuation



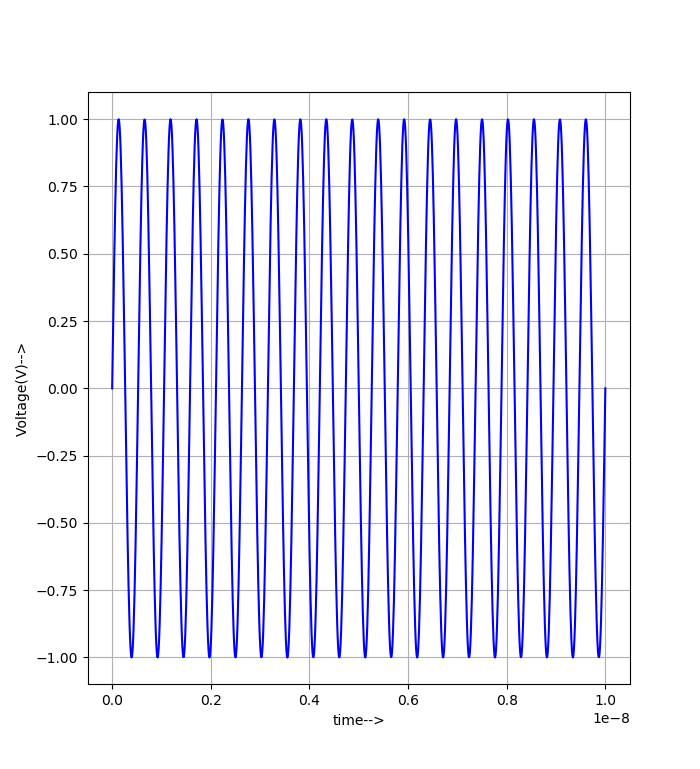
(1). **Input:**

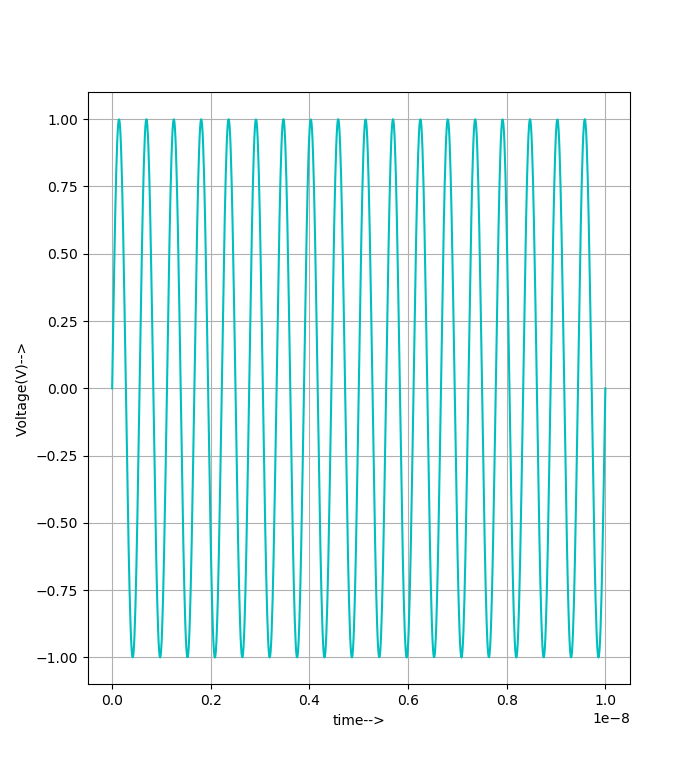
(a). Local Oscillator (LO)

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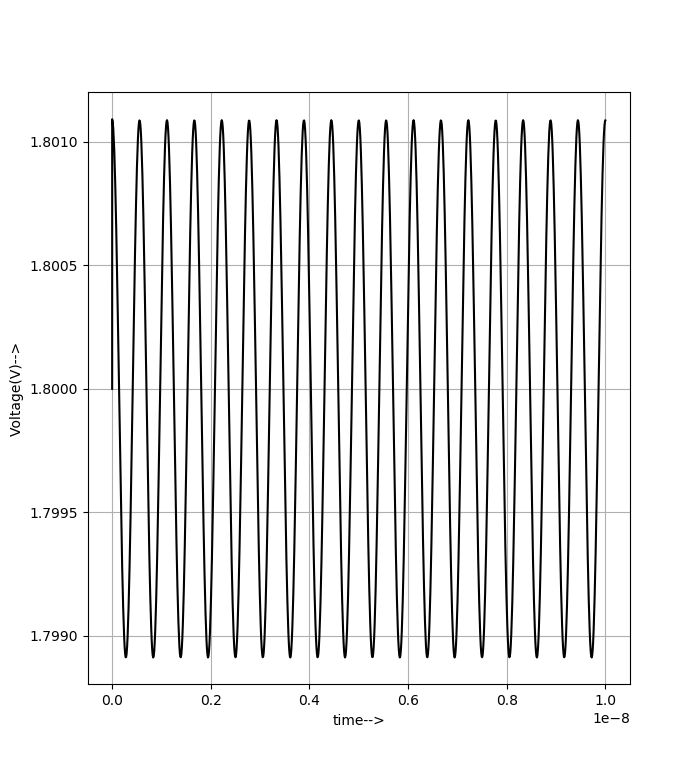


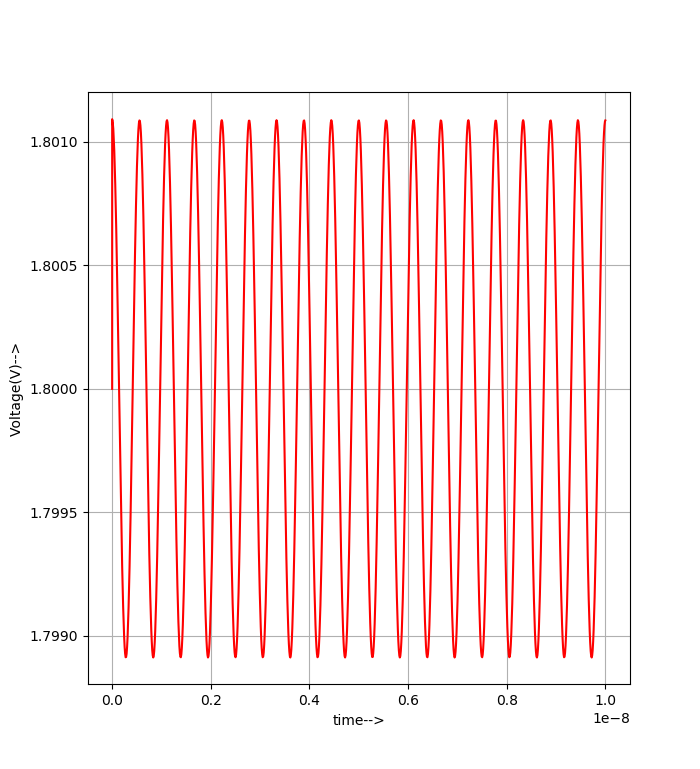
(B). Radio Frequency (RF)

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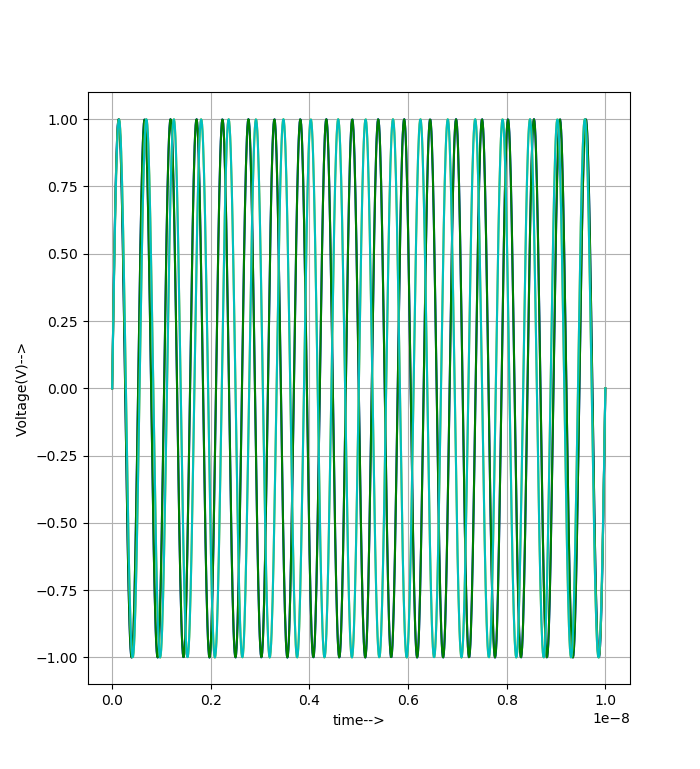
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**(2).Output:**

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**Input & Output:**

****

**Conclusions**

The design of a down-conversion Gilbert cell mixer using 65 nm CMOS technology demonstrates significant advancements in gain conversion and isolation. The

implementation of a new degenerating structure effectively improves linearity, making it an effective solution for modern communication applications.

**Research Paper**

**Discover** Electronics

**Review**

**Advances in active down‑conversion mixer linearity techniques: a comprehensive review**

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## Abstract

In the modern era, the demand for high-speed communication has led to a growing preference for higher bandwidth. However, in wideband scenarios, the presence of neighboring bands can introduce nonlinearity issues in mixers. The RF stage and Switching stage are identified as the primary contributors to nonlinearity in down-conversion mixers. This article presents a basic principle as well as circuit architectures of the mixer, including a performance parameters comprehensive review of linearity improvement techniques employed in down-conversion mixers. The paper categorizes various previously reported methods to enhance the linearity of the RF stage into five approaches: (1) MGTR/Derivative superposition (DS), (2) Complementary DS (CDS), (3) noise cancellation (NC), (4) post distortion (PD), and (5) feedforward or feedback approach.

These techniques aim to enhance the Second-order nonlinearity ( *gm*′ ) or third-order nonlinearity ( *gm*′′ ) of the RF stage.

Among these approaches, Noise Cancellation (NC) methods demonstrate superior optimization in terms of Conversion Gain, Linearity, and Noise Figure. Furthermore, to improve the linearity of the switching stage in mixers, the static and dynamic current injection methods can be employed. The objective of this review is to contribute to the advancement of linearity improvement techniques for wideband active down-conversion mixers, while also facilitating future research and development in this field.

**Keywords** Down-conversion mixer · Noise cancellation · Derivative superposition · Complementary derivative superposition · Linearity improvement

## 1 Introduction

The demand for fast data-rate wireless communication is experiencing rapid growth in today’s world, especially in urban areas, placing significant emphasis on the RF Front end (RFFE), which must operate across a wide range of frequencies [1]. Several receiver architectures are available for implementing wireless systems, including super-heterodyne, low IF, direct conversion, image rejection, and digital IF receivers [2]. Among these, the low IF architecture shown in Fig. 1 is a preferred solution for wideband applications due to its ability to eliminate DC offsets and the tendency to reduce the flicker (1/f) noise [3, 4].

Alkeshkumar Vaghela and Hasmukh Koringa both contributed equally to this article.

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**Fig. 1**

Direct

-

conversion

Receiver architectures for

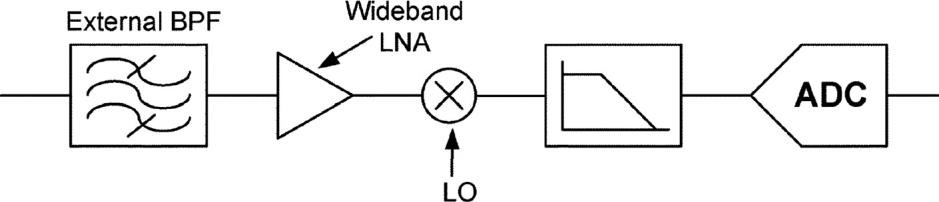
Ultra

-

Wideband (UWB) [

2

]



The RF Front End (RFFE) comprises several crucial elements, such as low noise amplifiers (LNA),down-conversion mixers, and oscillators (VCO). Among these components, the performance of the LNA - MIXER pair plays a pivotal role in the overall performance of the RFFE, including aspects like linearity, Noise Figure (NF), and Conversion gain. Therefore, it is essential to enhance the performance of the LNA–MIXER pair simultaneously to achieve significant improvements in the overall RFFE performance [5].

The upper limit of the dynamic range in the Radio Frequency Front-End (RFFE) system is determined by linearity [6], with the lower limit influenced by system noise. The Noise Figure (NF) of the mixer significantly impacts RF system performance, affecting both received and processed signals. Implementing mixers with CMOS technology ensures optimal performance, characterized by low power consumption and high integration density [7, 8].

The CMOS mixer can be divided into two types: active and passive. The active mixer utilizes a current signal for frequency conversion, while the passive mixer employs a voltage signal for the conversion. Passive mixers showcase advantages such as less flicker noise (1/f), superior linearity, and wideband properties compared to their active counterparts [5]. However, passive mixers require higher LO signal power for driving, leading to inherent conversion losses, poor reverse isolation, and potential issues with larger noise coefficients and troublesome IQ crosstalk. As a remedy, compensatory peripheral circuits become necessary for passive mixers.

On the flip side, active mixers demand less LO signal power, offer higher conversion gain ( *Gc* ) performance, and provide better isolation between RF, LO, and IF ports than passive mixers, enhancing noise rejection for subsequent circuit modules [9]. Nevertheless, they tend to exhibit lower linearity compared to passive mixers [2]. The choice between active and passive mixers in the design process must be made based on the expected performance index (Table 1). With the continuous improvement in mixer performance, most mixers now include modules based on the Gilbert doublebalanced mixer [10]. The active mixer consists of two types [11]:

• Switched Transconductance (Sw+Gm) Mixer: The mixers depicted in Fig. 2 utilize Switched Transconductance (Sw+Gm) technology, employing four CS MOSFETs ( *M*3–*M*6 ) within their RF input stage to create RF transconductance pairs. These mixers also feature an LO switching stage ( *M*1–*M*2 ) that operates differentially, modulating the bias current ( *IB*+*iRF* ) that passes through the RF transconductance pairs. Furthermore, they incorporate a load stage ( *RL* ) where periodically commutated RF signal current is transformed into an IF signal voltage. The Sw+Gm Mixer demonstrates superior thermal noise performance due to minimal noise from switching devices, making it advantageous for applications with lowvoltage requirements. This aspect is emphasized in an analysis detailed in [12], focusing on a mixer tailored for lowvoltage operation challenges. It achieves competitive performance at reduced supply voltages by employing switches tied exclusively to supply voltages. This design choice addresses gate-oxide reliability issues and minimizes voltage headroom requirements by employing two transconductors with cross-coupled outputs activated by switches, effectively competing with traditional mixers. Moreover, the integration of low-ohmic switches minimizes

Aspect

Active

mixer

Passive mixer

**Table 1** Comparison table of Advantages active mixers and passive mixers **Fig. 2** Double balanced mixer

(Sw+Gm) configuration voltage

Disadvantages drop, maximizing supply

High integration, small size

Low LO drive requirements

Integrated LO frequency multiplier

Good isolation

High conversion gain

Poor linearity and NF

Higher power consumption

Wide bandwidth

High dynamic range

Low noise figure

High port-to-port isolation

Limited flexibility in integration

High LO input power

High signal loss at the output

voltage headroom and Furthermore, [11]

enhancing

conversion

gain.

presents

a

mathematical

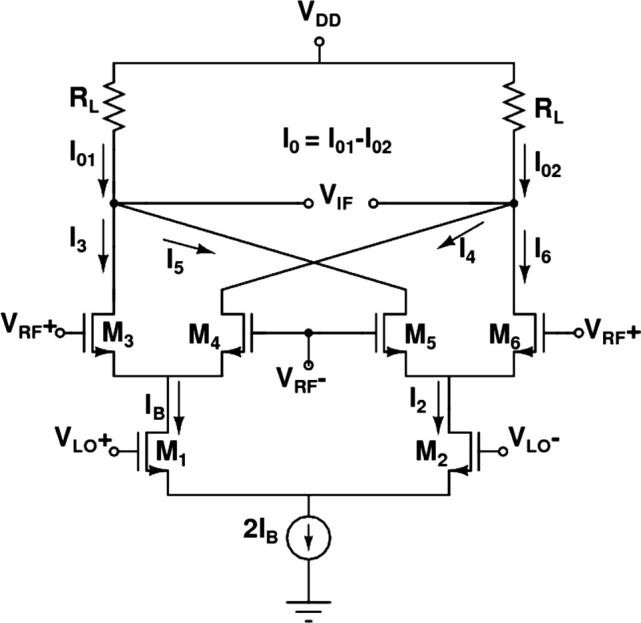
model

mechanisms

in

Switching

Transconductance (Sw+Gm) mixers, along with challenges



addressing flicker noise posed by parasitic capacitance at high frequencies (HF).

Additionally, in [13], the Sw+Gm mixer is evaluated for its high mixer common-mode rejection ratio (MCMRR). Recommendations from this analysis include utilizing sinusoidal LO driving for noise advantages and integrating an

inductor resonating structure to tackle operation frequency limitations due to tail parasitic capacitances. The paper also

discusses strategies for reducing flicker noise in mixers designed for direct-conversion receivers, such as incorporating a PMOS transconductance structure.

• Gilbert (Gm+Sw) Mixers: These mixers utilize LO switch pairs ( *M*3–*M*6 ) to modulate the RF current ( *IB*+*iRF* ) from an RF transconductance stage(*M*1–*M*2 ), controlled by a large LO signal. This process completes the frequency conversion from RF to IF. The configuration of this Gilbert cell mixer is illustrated in Figs. 3 and 4. The operational aspects of this mixer type are extensively discussed in [14].

**Fig. 3** Double balanced mixer

![](data:application/octet-stream;base64,)![](data:application/octet-stream;base64,)

(Gm+Sw) configuration [19] **Fig. 4** Single balanced mixer configuration [19]

Table 2 presents a discussion comparing Gilbert (Gm+Sw) Mixers with Switched Transconductance (Sw+Gm) Mixers. Moreover, as the number of cascaded stages increases, there is

a corresponding increase in nonlinearity and noise, leading to various effects such as harmonic distortion, intermodulation, cross-modulation, gain compression, and desensitization [4]. Therefore, the role of the mixer is crucial as it directly influences the linearity (IIP2, IIP3), noise figure (NF), and conversion gain ( *Gc*).

Designing down-conversion active mixers for wideband applications requires special attention to linearity due to 2nd order intermodulation (IM2) and 3rd order intermodulation (IM3) occurring within the frequency bands [2]. Therefore, ensuring high linearity is vital to mitigate the impact of these intermodulation distortions in wideband scenarios. The Active double-balanced mixer consists of 3 stages [10]:

1. RF transconductance stage ( *M*1–*M*2 ): This stage converts the RF voltage signal into current, utilizing a biased differential pair that functions as the RF transconductance amplifier.
2. Switching Stage ( *M*3–*M*6 ): Driven by a local oscillator signal (LO), the switching stage ( *M*3–*M*6 ) is tasked with performing the mixing operation.
3. Load/IF Stage ( *RL* ): This stage plays a dual role by converting current to IF voltage and serving as the load for the mixer. Additionally, it functions as the intermediate frequency (IF) amplifier.

The operation of the active mixer is extensively discussed in [14]. The double-balanced structure provides advantages such as LO rejection, rejection of even-order distortion products, higher conversion gain ( *Gc* ), and improved noise performance. However, it exhibits considerably worse linearity [5, 15] and flicker noise performance [12].

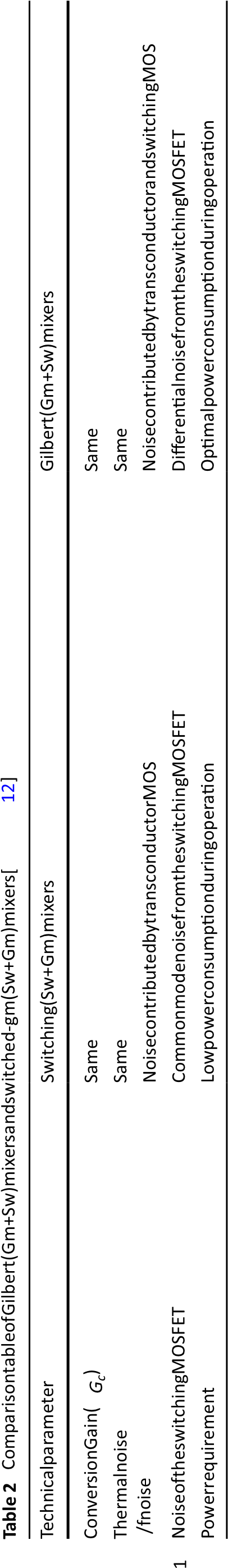
Flicker noise (1/f noise), becomes a significant consideration especially when mixers are used in Direct Conversion Receivers (DCR) applications. This type of noise manifests in all three stages of the mixer: the RF stage, the load stage, and particularly in the switching MOS devices.

RF Stage Flicker noise is up-converted into LO frequency and that does not appear at the baseband [14]. Properly sizing active load devices or using poly resistors in the mixer can minimize flicker noise in the load stage. major concern about the Switching noise: Mismatches in the switching pair contribute to flicker noise which is extensively discussed in [16]. Various techniques have been reported to reduce flicker noise in CMOS active mixers, such as negative Impedance [16], dynamic current injection [17] and RF leakageless static current bleeding with resonating inductors [18]. These methods aim to enhance mixer performance, particularly in applications demanding low noise and high linearity for the Direct Conversion Receivers (DCR) applications.

## 2 S ources of non‑linearity in mixer

The active mixer consists of 3 stages: RF transconductance, switching, and load/IF. Non-linearity in mixers can be traced back to two main stages:

1. RF transconductance stage: The primary source of non-linearity in this stage is attributed to the MOSFET ( *M*1–*M*2 ), as discussed in Sect. 2.1.



1. Switching stage: The non-linearity of the mixer is influenced by the non-ideal switching behavior exhibited by MOSFETs ( *M*3–*M*6 ), as discussed in Sect. 2.2.

These two stages, RF transconductance and switching play significant roles in the occurrence of non-linearity in the active mixer, and their effects are thoroughly explored in the respective sections of the paper.

### *M M*

#### 2.1 T ransconductance stage non‑linearity (RF stage 1– 2)

Active mixer gets an amplified version of the input from LNA ( *vRF* ) and converts it into current ( *iRF* ) through the of RF MOSFET ( *M*1–*M*2 ) as shown in Fig. 3.

The non-linearity introduced by the RF stage originates from two sources [20, 21]:

1. Transconductance ( *gm* ): Converts the linear input ( *vRF* ) into non-linear output current ( *iRF*).
2. Non-linear output conductance ( *gds* ): The effect of this component becomes noticeable when there is a high output voltage swing at the drain node of ( *M*1–*M*2).

The non-linear behavior exhibited by the RF stage ( *M*1 ), as illustrated in Fig. 4, can be modeled using a power series, with the higher-order coefficients being omitted.

= 1 + *gm* 1 2 + *~~gm~~*~~1~~ 3 + ~~(1~~) *iRF gm vRF* 2! *vRF* 3! *vRF*

where

*𝜕 IDS*  *𝜕*2*IDS*  *𝜕*3*IDS*

*gm*1 = *𝜕 VGS* , *gm*1 = *𝜕 VGS*2 , *gm*1 = *𝜕 VGS*3 (2)

1 1 *IIP*3= ′ 1 ′′ (3)



|||

1

|||||

where *gm* = Transconductance of MOSFET *M* and *iRF* = Output current of MOSFET *M* .

Figure 5 illustrates the simulated profile of 2nd order non-linearity ( *gm*1 ) and 3rd order non-linearity ( *gm*1 ) for the RF stage ( *M*1 ). The presence of non-zero *gm*′ and *gm*′′ of the RF stage degrades the IIP3 (third-order intercept point) performance of the mixer according to Eq. 3. Consequently, different techniques have been reported in the literature [20, 21] to mitigate or nullify the effects of *gm*′ and *gm*′′ of the RF stage ( *M*1 ). These techniques include (1) Multiple Gated Transistor (MGTR)/Derivative Superposition (DS) [15, 22–24], (2) Complementary Derivative Superposition (CDS) [25–27], (3) Noise/ Distortion cancellation (NC) [24, 28–32], (4) Post Distortion (PD) [33, 34], and (5) Feedback Approach [35].

![](data:application/octet-stream;base64,)**Fig. 5** RF stage MOS ( *M*1 ) transconductance profile (gpdk 90nm CMOS process,

W/L = 120/100, Vds = 1 Volt)

[19]

#### 2.2 Switching stage non‑linearity ( *M*3–*M*4)

The mixing process takes place in the switching stage ( *M*3–*M*4 ), where the current ( *iRF* ) is combined with the LO signals, as depicted in Fig. 4. The desired condition for an ideal mixing operation is to have one MOSFET in the switching stage in the ON state while the other MOSFET is in the OFF state. However, in practical scenarios, achieving this ideal condition is not possible due to the sinusoidal nature of the Local Oscillator (LO) signal. The sinusoidal LO signal causes both the switching stage MOSFETs to be turned ON simultaneously for a certain period [19]. To ensure that both the RF stage

( *M*1 ) and the switching MOSFETs ( *M*3–*M*4 ) remain in the saturation regime, the voltage at the drain node of the switching MOSFETs must be sufficiently high. If the voltage at the drain node of the switching MOSFETs is not adequately high, the switching MOSFETs ( *M*3–*M*4 ) will operate in the triode region, introducing non-linearity into the switching stage [36].

The small signal current ( *i*01 ) of an *M*3 is a function of the instantaneous values of the transconductance stage’s output current ( *iRF* ) and Local oscillator voltage *VLO*(*t*) shown in Fig. 6. This relationship can be represented by the equation:

*I*01 + *i*01 = *Function* (*VLO*(*t*), *iRF* + *IB*). (4)

In the equation above, *IB* and *i*01 represent the DC currents resulting from the biasing conditions Comparison table of Gilbert (Gmat the RF stage and the output of the LO stage, respectively. The third-order Taylor expression of Eq. 5

*i*01 = *q*1(*t*)*iRF* + *q*2(*t*)*iRF*2 + *q*3(*t*)*iRF*3 (5)

where

*𝜕 F 𝜕* 2*F 𝜕* 3*F q*1(*t*) = *𝜕* , *q*2(*t*) = 2 *q*3(*t*) = *𝜕 I*3 (6)

*IB 𝜕 IB B*

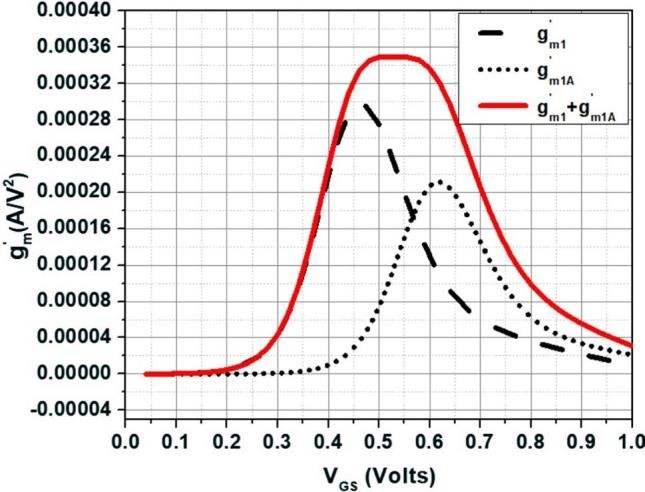
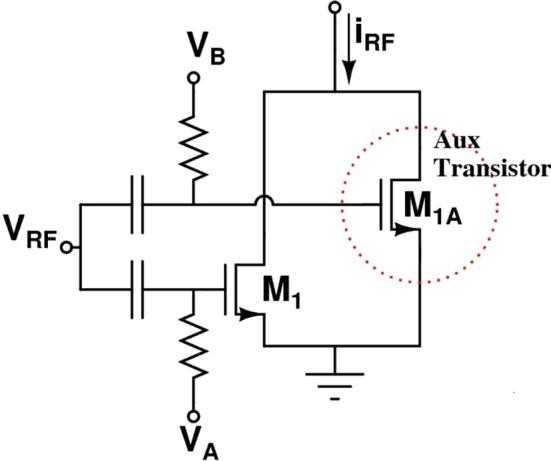
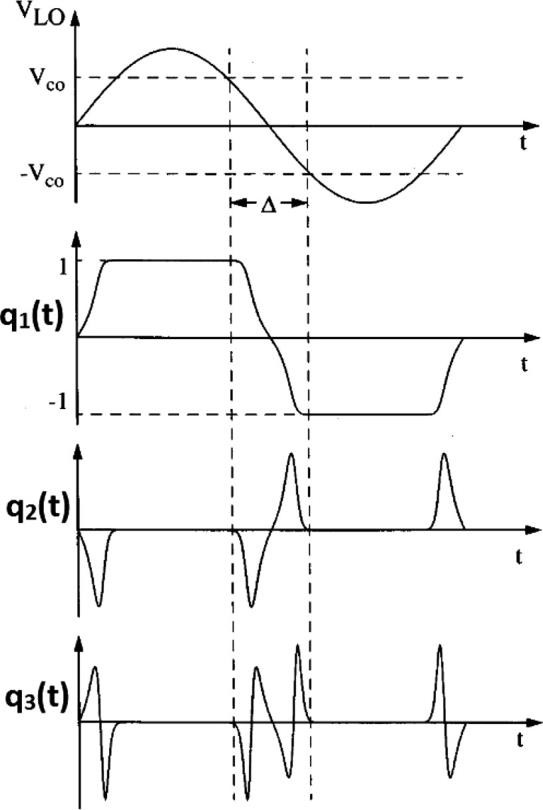
Periodic waveforms of non-linearity coefficients are shown in Fig. 6. For sinusoidal LO, will be non-zero for the time interval

(Δ) in which either *M*2 or *M*3 enters in triode regime before the other MOSFET turns OFF. This deteriorates the linearity of mixer [19].

**Fig. 6** Typical waveforms of

=1

V



(*q*1(*t*), *q*2(*t*)*and q*3(*t*)) [19]

**Fig. 7** Derivative superposition technique

**Fig. 8**

Simulation result of *gm*′ in

GPDK 90nm

CMOS process,

(*W*∕*L*)1 =

165∕100 ,

(*W*∕*L*)1*A* =

120∕100 , *Vds*

## 3 Linearization methods

In an active CMOS mixer, the non-linearity of the RF transconductor stage MOSFETs ( *M*1–*M*2 ) can be mitigated by canceling out the effects of *gm*′ and *gm*′′ . Similarly, to enhance the linearity of the switching stage, it is important to maintain a sufficient voltage at the drain node of ( *M*3–*M*4 ) to prevent these MOSFETs from entering the triode region [17], as well as to keep *M*1 and *M*2 in the saturation regime.

Sections 3.1 to 3.4 discuss various methods for boosting the linearity of the RF transconductor stage. On the other hand, Sect. 3.5 specifically focuses on techniques to enhance the non-linearity of the switching stage.

### 3.1 Multiple gated transistor (MGTR)/derivative superposition (DS)

The simulations of *gm*′ 1 and *gm*′′1 for the RF stage MOSFET ( *M*1 ) are depicted in Fig. 5. The profile of *gm*′′1 exhibits both a positive peak and a negative peak. In order to mitigate the impact of *gm*′′1 , an auxiliary MOSFET ( *M*1*A* ) is introduced and connected in parallel with *M*1 , as depicted in Fig. 7. The Simulation results presented in Figs. 8 and 9. By precisely adjusting the biasing voltage for the weak inversion region and sizing of the auxiliary MOSFET ( *M*1*A* ), it is possible to achieve cancellation by overlapping the negative peak of *gm*′′1 for *M*1 and the positive peak of *gm*′′1*A* for *M*1*A* . Consequently, the overall value of *gm*1 +*gm*1*A* becomes zero as shown in Fig. 9, effectively eliminating the undesired non-linearity caused by *gm*′′1 . This cancellation technique helps in enhancing the linearity of the RF stage by minimizing the distortions introduced by *gm*′′1.

However, utilizing a single auxiliary MOSFET ( *M*1*A* ) has limitations in terms of achieving a corrected flat zone due to the asymmetrical positive and negative properties. To extend the flat zone and improve linearity, multiple auxiliary

![](data:application/octet-stream;base64,)**Fig. 9** Simulation result of *gm*′′ in GPDK 90nm CMOS process, (*W*∕*L*)1 = 165∕100 ,

(*W*∕*L*)1*A* = 120∕100 , *Vds* =1

V

MOSFETs can be connected in parallel with *M*1 . However, this approach leads to gain degradation due to increased parasitic capacitance [20]. The *gm*′ 1 and *gm*′ 1*A* profiles for transistors *M*1 and *M*1*A* exhibit only a positive peak as depicted in Fig. 8. Biasing *M*1 and *M*1*A* to mitigate 3rd order non-linearity reduces *gm*′′ but introduces 2nd order non-linearity in the form of increased total *gm*′ ( *gm*1 +*gm*1*A* ). Consequently, this trade-off leads to a degradation in the 2nd order input intercept point (IIP2), negatively impacting the linearity performance.

Limitations of using an auxiliary MOSFET in the weak inversion region in the Derivative Superposition (DS) method include (a) Limited frequency range of operation, (b) Inability to handle large input signals, and (c) Sensitivity to PVT variations (process, voltage, and temperature) for linearity improvement.

The Derivative Superposition (DS) technique has been employed in various literature [15, 22–24, 37, 38] to linearize the *gm*′′1*A* of the CS transconductance stage MOSFET *M*1 , either on its own or in combination with other techniques.

### 3.2 Complementary derivative superposition (CDS)

Derivative superposition (DS) linearization approach to improve the IIP3 but degrade the IIP2 performance of the mixer. To address this issue, the auxiliary NMOS ( *M*1*A* ) can be replaced with a PMOS ( *M*1*P* ) in the Complementary Derivative Superposition (CDS) method [39] as shown in Fig. 10. Output current ( *iRF* ) can be written as,

**Fig. 10** Complementary derivative superposition technique

![](data:application/octet-stream;base64,)![](data:application/octet-stream;base64,)

**Fig. 11** Simulation result of *gm*′ in GPDK 90nm CMOS process,

(*W*∕*L*)1 = 165∕100 ,

(*W*∕*L*)1*A* = 120∕100 , *Vds*

=1 V

![](data:application/octet-stream;base64,)**Fig. 12** Simulation result of *gm*′′ in GPDK 90nm CMOS process, (*W*∕*L*)1 =

165∕100 , (*W*∕*L*)1*A* = 120∕100 , *Vds* =1 V

*iRF* = (*gm*1 + *gm*1*p*)*vgs* +(*gm* 1 − *gm* 1*p*)*vgs*2 +(*gm*1 + *gm*1*p*)*vgs*3 (7)

From Eq. 7, the total *gm* will increase to ( *gm*1 + *gm*1*p* ). *gm*′ 1 of *M*1 and *gm*′ 1*p* of *M*1*P* are added with opposite signs, resulting in an overall *gm*′ of zero, while *gm*′′1 of *M*1 and *gm*′′1*p* of *M*1*P* are subtracted with the same sign, resulting in a reduction in *gm*′

, as shown in Figs. 11 and 12. A cancellation window for *gm*′′ is wider for DS compared to CDS. Therefore, the enhancement in IIP3 is not as substantial as that observed in Derivative Superposition (DS).

In the Complementary DS (CDS) technique, the optimal biasing of *gm*′ 1 and *gm*′′1 does not coincide. Consequently, two options are available: *gm*′′1 and *gm*′′1*p* can be matched to achieve a good 3rd order input intercept point (IIP3) while partially cancelling *gm*′ 1 , and *gm*′ 1*p* can be matched to attain the optimal 2nd order input intercept point (IIP2).

The CDS technique is used to linearize the transconductance stage of the down-conversion mixer, which is operated for

−

Band-1 (3.1 4.8 GHz) of the UWB mixer [25]. In [26] and [27], various versions of CDS are discussed which can be used in the mixer to improve the IIP3 and IIP2. *gm*′′1 of the RF stage of an active mixer can be canceled by applying a voltage to the bulk terminal, called the Gate-Bulk Interaction Technique [40, 41].

### 3.3 Post distortion (PD)

The Post-distortion method, as compared to the DS method, employs an auxiliary MOSFET connected at the drain of the RF stage MOSFET. This auxiliary MOSFET is utilized to cancel out the *gm*′ and *gm*′′1 characteristics of the RF stage MOSFET ( *M*1 ) in mixers [33].

![](data:application/octet-stream;base64,)**Fig. 13** Common Gate (CG)

Post-distortion [33]

![](data:application/octet-stream;base64,)**Fig. 14** Common Source (CS)

Post-distortion [33]

Figures 13 and 14 illustrate the implementation of CG and CS post-distortion, with MOSFETs *M*1 and *M*2 degenerated by resistance ( *Zs* ). The increased parasitic capacitance reduces conversion gain ( *Gc* ) at higher frequencies, mainly due to Cgs of the LO MOSFET ( *M*3 - *M*6 ) as shown in Fig. 3. To counteract the effects of parasitic capacitance at the source node of the switching stage and ensure a consistent conversion gain ( *Gc* ) across a wider frequency range, inductor *L*1 (depicted in Fig. 13) and inductor *L*2 (depicted in Fig. 14) are introduced between the LO and RF stages. Recent research, as reported in [42], proposes the utilization of Active Inductor (AI) instead of simple inductors, offering enhanced bandwidth.

The implementation of CG and CS post-distortion are shown in Figs. 13 and 14, where MOSFET *M*1 and *M*2 is degenerated by resistance ( *Rs* ). For CG implementation, current flowing through the *M*1 and *M*1*Q* can be written as,

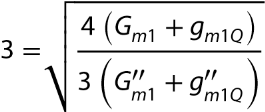
*iRF* = *Gm*1*vRF* + *Gm* 1*vRF*2 + *Gm*1*vRF*3 (8)

where,

*gm*1

*Gm*1 = (9) 1+*gm*1*Zs*

|  |  |
| --- | --- |
| *i*1*Q* =*gm*1*QvRF* + *gm* 1*QvRF*2 + *gm*1*vRF*3 | (10) |
| *iRF* = *i*1 + *i*1*Q* =(*Gm*1 + *gm*1*Q*)*vRF* + (*Gm* 1 + *gm* 1*Q*)*vRF*2 + (*Gm*1 + *gm*1*Q*)*vRF*3 | (11) |

*IIP* (12)

By observing Eqs. 11 and 12, it becomes evident that the linearity (IIP3) can be enhanced by reducing the term ( *gm*′′1 + *gm*′′1*Q* ). To achieve this, proper biasing of the transistors ( *M*1 ) and ( *M*1*Q* ) is required.

However, the post-distortion (PD) method offers advancements in 2 key aspects:

1. The auxiliary MOSFET is connected to the output of the main MOSFET rather than directly to the input. This minimizes the impact on input matching, ensuring better overall performance.
2. All MOSFET operates in saturation, providing a more robust cancellation of distortions.

These advancements make the post-distortion method a more suitable technique for canceling out *gm*′ 1 and *gm*′′1 in the RF stage MOSFET ( *M*1 ). The post-distortion method involves operating both MOSFETs *M*1 and *M*1*Q* in the saturation region, which results in no degradation of the conversion gain ( *Gc* ) and noise figure compared to the DS and CDS methods.

### 3.4 Noise/distortion cancellation

Noise is a crucial consideration in mixer design, with the Noise Figure (NF) often being relatively high. Various circuit topologies are employed to minimize both flicker [16] and white noise in CMOS mixers. In [43], a novel RF CMOS Gilbert mixer is proposed to enhance NF. This mixer utilizes a PMOS switching circuit with an inductor to sharpen switching transitions and reduce flicker noise at the switching stage. Additionally, in [24, 28–31, 44], circuit topologies are utilized to minimize RF stage noise in CMOS down-conversion mixers. The principle of noise cancellation is depicted in Fig. 15, with *Rs* representing the source impedance. The concept of noise cancellation [45] involves the identification of two nodes (X and Y) in the RF stage. At these nodes, the signal exhibits opposite polarities, while the noise from the input transistor exhibits the same polarity. When nodes X and Y satisfy this condition, their voltages can be appropriately scaled and combined, resulting in the addition of signal components and cancellation of noise components.

Two topologies can be utilized for noise cancellation in the RF stage of the Mixer: (1) Common Gate (CG)-Common Source (CS) topology (2) Common Source (CS) topology with feedback (resistive).

#### 3.4.1 CG‑CS topology

The CG-CS approach offers two possible output configurations, namely the differential output [30] and the single-ended output [31, 46], as illustrated in Figs. 16 and 17 respectively. The utilization of a differential output in the differential approach eliminates the requirement for a balun at the input of the RF stage. However, there are various trade-offs to consider among gain, IIP3 (3rd order intercept point), and noise figure. To mitigate these trade-offs, one can introduce an additional NMOS ( *M*1*F* ) to convert the differential output to single-ended output as shown in Fig. 17. This conversion helps in eliminating the trade-offs associated with the differential approach.

In the CG-CS noise cancellation approach, the input CG MOSFET ( *M*1*E* ) generates a noise voltage with opposite polarity at nodes X and Y, while the input signal remains in phase, as depicted in Figs. 15 and 16 respectively. To combine the

**Fig. 15** Conceptual representation of noise cancellation technique

![](data:application/octet-stream;base64,)![](data:application/octet-stream;base64,)

**Fig. 16** CG- CS approach

differential output [30]

![](data:application/octet-stream;base64,)**Fig. 17** CG-CS approach single ended output [31] input signal and effectively cancel

the noise (channel, thermal) and distortion generated by the input MOSFET ( *M*1*E* ) at the output, it is necessary for the gain of the CG stage ( *M*1*E* ) and the

CS stage ( *M*1 ) to be equal. This condition results in the Noise Cancellation Condition for differential output as,

*gm*1*ER*1 = *gm*1*R*2 (13)

For single-ended output,

*gm*1*FR*1 = *gm*1*RS* (14)

In the CG-CS topology, the RF signal is applied to the source of the CG MOSFET ( *M*1*E* ). The impedance seen at the source

) is approximately  *m*11*E* ) , allowing for the straightforward achievement of wideband input matching by

of ( *M*1*E* (*g*

appropriately setting the value of ( *g* ). Limitations:

*m*1*E*

1. The inclusion of an additional MOSFET ( *M*1*F* ) in the CG-CS single-ended output configuration of Fig. 17 leads to increased noise compared to the CG-CS differential configuration.
2. While the noise and distortion originating from ( *M*1*E* ) are effectively eliminated by the noise cancellation (NC) methods, it is important to note that the presence of ( *M*1*F* ) and ( *M*1 ) can still introduce residual noise and distortion. These residual factors can potentially impact the linearity performance of the mixer.

#### 3.4.2 CS‑resistive feedback topology

This approach, as shown in Fig. 18, replaces the CG input MOSFET ( *M*1*E* ) with a CS MOSFET ( *M*1*C* ), distinguishing it from the CG-CS topology. As discussed in the CG-CS topology, the noise and RF signal from the input MOSFET ( *M*1*C* ) generate opposite polarity noise voltage at Node X and an in-phase RF signal at Node Y. Noise cancellation condition for CSResistive feedback topology can be written as,

**Fig. 18** CS Resistive feedback [29] ![](data:application/octet-stream;base64,)

*gm*1*RS* = *gm*1*D*(*RS* +*RF*) (15)

This approach suffers from insufficient output impedance, making it unsuitable for direct integration as the RF stage in the down-conversion mixer. However, in [29], an enhanced resistive feedback noise cancellation approach is presented. This modification involves substituting the source follower ( *M*1*D* ) with a common-gate (CG) amplifier and replacing the input RF stage with a complementary resistive feedback amplifier ( *M*2*NC* , *M*2*PC* and *RF* ). Additionally, the output is converted into a complementary output stage, as depicted in Fig. 19. This modification results in additional feed-forward signal amplification, leading to increased gain and reduced noise in the circuit. Furthermore, the modified approach exhibits a desirable characteristic of high output impedance, making it well-suited for use as an RF stage in the downconversion mixer. The noise cancellation condition for Fig. 19 can be modified as given in [29].

(*gm*1*N* +*gm*1*P*)*RS* = *gm*1*D*(*RS* +*RF*) (16)

where, *gm*1*N* , *gm*1*P* , *gm*1*D* are the transconductance of MOSFET *M*1*N* , *M*1*P* and *M*1*D* respectively. The output complementary stage allows the cancellation of distortion from *M*1*N* and *M*1*D* effectively by *M*1*P* , which is biased in the weak inversion region and carefully optimized around the sweet spot to minimize *gm*′′1*N* and *gm*′′1*D* . This optimization leads to a noticeable improvement in IIP3. Furthermore, to remove the impact of second-order interaction on IIP3, complementary configurations are proposed in [28]. The CG-CS noise cancellation approach for the RF stage in a mixer is superior to the CSResistive approach, especially in situations where wideband (WB) input matching, higher conversion gain ( *Gc* ), and low Noise Figure (NF) are required.

### 3.5 Current injection

The methods mentioned above, such as noise cancellation (NC), post-distortion (PD), CDS (complementary DS), and DS

(Derivative Superposition), are utilized to eliminate *gm*′ 1 and *gm*′′1 in the RF STAGE *M*1 , resulting in an enhancement of IIP3.

**Fig. 19** Modified noise cancellation approach [29]

![](data:application/octet-stream;base64,)![](data:application/octet-stream;base64,)

**Fig. 20** Static current injection method [17]

**Fig. 21** Dynamic current injection method [17] ![](data:application/octet-stream;base64,)

Moreover, as explained in Sect. 2.2, the mixer’s IIP3 is affected by the time interval ( (Δ) ) when one of the switching

MOSFETs enters the triode region, leading to deterioration in the linearity of the mixer, as depicted in Fig. 6. To prevent the switching MOSFETs from entering the triode region, it is necessary to maintain a sufficient voltage at the drain node of *M*3 and *M*4 . To accomplish this, both static and dynamic current injection approaches have been proposed in [17], as illustrated in Figs. 20 and 21.

Minimum node voltages at X and Y can be written as,

*VX*,*Y*,(*min*) =*Vov*1 +1+*Vov* 3,4 (17) where, *Vovn* = Overdrive voltage of MOSFET *Mn*.(n = 1,2,3,4)

#### 2 *V*

(18)

*ConversionGainmax* = *𝜕 VRmaxov*1

The implementation of static current injection involves the connection of PMOS transistors *M*7 and *M*8 across the load resistor ( *RL* ), as depicted in Fig. 20. To ensure that the external current sources ( *M*7 and *M*8 ) remain in saturation during LO zero crossings, it is necessary to maintain a sufficient voltage across the load resistor.

*VRmaximum* =*Max*(*VRL*)=*VDD* −*VX*,*Y*,*Min* (19)

The static current injection method [17] involves the continuous injection of a constant current throughout the entire duration of the LO signal. While this approach provides only a limited improvement in conversion gain, it helps mitigate signal compression at the output. To further enhance conversion gain and reduce signal compression, dynamic current injection is utilized. In this method, the current is injected at the nodes X and Y using a PMOS ( *M*7 - *M*10 ) cross-coupled pair, as depicted in Fig. 21. Additionally, dynamic current injection eliminates the voltage across the *RL* at the zero crossing LO signal.

Furthermore, the current bleeding/Injection method also enhances flicker (1/f) noise performance, which involves reducing the current in the switching stage to decrease the height of noise pulses [18]. This reduction is achieved by introducing additional bias current ( *Ibld* ) at the source node of the switching stage, as illustrated in Fig. 22. The current bleeding technique aims to lower the bias current of the LO switches. However, this action leads to an increase in the impedance of the LO switches as observed from the RF stage. Furthermore, RF leakage current enters the bleeding circuit, resulting in reduced conversion gain ( *Gc* ) and allowing more RF current to be diverted by the parasitic capacitance ( *Cp* ) at the node between the LO switches and the RF transconductance stage. Minimizing *Cp* is crucial for indirectly reducing flicker noise [16]. To achieve this, using smaller device sizes for the LO switches is appropriate, although it may increase intrinsic flicker (1/f) noise. Another proposed technique, dynamic current bleeding, enhances flicker-noise performance by injecting a dynamic current equal to the bias current of the LO switches only during LO switching events [16].

## 4 R esearch scope, challenges and future direction

### 4.1 Research Scope and Challenges

In the field of communication technology, Ultra-Wideband (UWB) devices have experienced rapid growth across diverse domains, including medical applications, short-range distance communication, positional tracking, and beyond [2, 3, 15, 21]. The extensive adoption of UWB underscores the need for continuous advancements in downconversion mixer research, offering both opportunities for future developments and significant challenges.

1. Challenges in mixer design for specific applications: Creating a down-conversion mixer tailored for a specific job is quite a challenge. It needs to perform well in areas like conversion gain ( *Gc* ), Noise Figure (NF), Linearity (IIP3, IIP2, P1dB), Port-to-Port Isolation, and more [10]. Achieving this optimal performance depends on how well we design and optimize CMOS mixers. However, this task comes with its share of difficulties, such as managing extra flicker noise, reducing LO port leakage, controlling high power consumption, and solving other tricky problems. Designing CMOS mixers is like solving a complex puzzle with many different elements that need to be just right. It’s not just about making something that works; it’s about making something that works well while navigating through all these challenges [10].

![](data:application/octet-stream;base64,)**Fig. 22** Concept of current bleeding

1. Growing demand for bandwidth and research focus: In recent years, the surge in demand for expanded bandwidth has propelled intensified research efforts in multiband mixers [10, 47]. The exploration of Multiband or Wideband mixers exposes challenges associated with nonlinearity stemming from neighboring bands. Consequently, the pursuit of enhanced linearity, particularly concerning 2nd and 3rd order non-linearity, has become a noteworthy and actively researched domain in the realm of multiband mixers.
2. Linearization techniques and ongoing challenges: This review article delves into various linearization techniques, providing a thorough analysis and detailed comparisons. Table 3 encapsulates a comprehensive overview of reported linearization techniques for down-conversion mixers. Notably, challenges persist in achieving an optimal balance. The Capacitive feedback approach [37] achieves an Average Value of IIP3 of 20.5 dBm, but at the expense

of noise performance (NF = 16.9 dB). Despite advancements, challenges linger, as evidenced by higher Noise Figure (NF) ranging from 11 to 14 dB in methods like CDS and DS/MGTR [15, 22, 23].

### 4.2 Future direction

1. Optimizing down-conversion mixer parameters:
   1. Designing a down-conversion mixer for a specific application with optimal parameters like conversion gain ( *Gc* ), Noise Figure (NF), Linearity (IIP3, IIP2, P1dB), Port-to-Port Isolation, and more [10]. Using gm/ID methods for downconversion mixers [48, 49] to optimize CMOS mixers.
2. Addressing challenges through innovative techniques:
   1. Methods like noise cancellation have been applied in the context of mixer design [31, 28, 29]. Although these strategies show positive results in aspects such as IIP3, conversion gain ( *Gc* ), and noise figure (NF), obstacles still **Table 3** Comparison of different linearization methods for the mixer

Ref.

RF BW (GHz)

IF BW (MHz)

Conversion DSB NF (

dB) gain

)

dB

(

IIP3 (dBm)

IIP2 (dBm)

Power diss. (mW)

Process (nm)

Key aspects

[15] 3.4−6.8 10 7.2−4.3 13.9−14.4 2–3 \*NM 2.9 180 MGTR

1. 2.4 \*NM 20.3 15 20.3 10.6 5.8 180 MGTR +

IM2

Injection

1. 0.8–5 50 9.8 11.53 11.83 57.3 13.95 65 DS +

IM2

Injection

1. 0.5−3.1 10 15 6.7 9.5 (Avg) \*NM 13.9 90 DS + NC
2. 3.1–4.8 300 12 13 24 81 3 130 CDS

[28]0.5−6.5 250 153.9−4.9 3.1–4.8 \*NM 7.2 65 CDS + CS NC [29]0.5−5.8 250 15 4.2 7.3–2.5 \*NM \*NM 130 CS NC

with Linearization

1. 1–9 50 19.2 8.4 (\*\*SSB NF) 0 \*NM 6.9 28 CG-CS NC

with \*D/O

1. 1−5.5 250 17.5 3.9 0.84 \*NM 34.5 130 CG-CS NC with \*S/O

[33] 5 \*NM 15.33 16.39 11.04 \*NM 1.53 180 CG-CS NC

with \*D/O

& PD

[35] 0.9–5 50 11.3 16.9 20.5 (Avg.) \*NM 3.5 65 Capacitive

Multiple

Feedback

[17]0.5−6.5 300 10 13 9.52 \*NM 4.5 130 Dynamic

Current

Injection

\*D/O=Differential Output, S/O=Single Ended Output, NM=Not Mentioned

\*\*SSB NF = DSB NF + 3 dB (SSB NF = Single Sideband NF) (DSB = Double Sideband NF) [14] exist. The challenge lies in achieving simultaneous enhancements in both IIP3 and IIP2 at the RF stage while addressing signal compression at the IF stage, presenting a substantial hurdle. This emphasizes the possibility of future improvements to enhance the overall performance across the Wideband (WB) spectrum.

(c) Incorporating innovative techniques from LNA architectures:

• Incorporating inventive methodologies from various Low-Noise Amplifier (LNA) architectures into mixers has the potential to augment performance. The utilization of various gain (gm) boosting techniques at the Common Gate (CG) stage [29, 30] can diminish the matching inductor size ( *Lin* ) and enhance matching. The integration of this improved LNA with a down-conversion mixer shows promise for enhancing linearity at the RF stage. Exploring additional techniques like inductive peaking [31, 50], active inductors [42], bulk LO injection, etc., in mixer design aims to widen the bandwidth. It’s essential to acknowledge that these methods may introduce additional parasitic capacitance. Subsequent research in this field could focus on layout optimizations to further refine and propel these concepts.

## 5 Conclusion

This article has explored various linearity improvement methods for CMOS Active current commutating mixers. The investigation involved considering trade-offs between linearity, conversion gain, and power dissipation. The use of DS and CDS techniques proved effective in enhancing the linearity of the RF stage ( *gm*′ and *gm*′′ ), but it led to a degradation in the Noise Figure. To further improve IIP3, IIP2, and *P*1*dB* in the RF stage, noise cancellation techniques in combination with linearization methods such as DS, CDS, or post-distortion can be applied simultaneously. Additionally, dynamic current injection can be implemented to enhance the linearity of the switching stage. By employing linearization techniques at both the switching and RF stages of the mixer, better overall linearization performance can be achieved. These findings contribute to advancing linearity techniques for CMOS Active current commutating mixers and guide the design of high-performance and linear mixers in practical wideband applications.

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